

# 74HC258

Quad 2-input multiplexer; 3-state; inverting

Rev. 04 — 14 April 2008

Product data sheet

## 1. General description

The 74HC258 is a high-speed Si-gate CMOS device and is pin compatible with low power Schottky TTL (LSTTL). The 74HC258 is specified in compliance with JEDEC standard no. 7A.

The 74HC258 has four identical 2-input multiplexers with 3-state outputs, which select 4 bits of data from two sources and is controlled by a common data select input (S).

The data inputs from source 0 (1I0 to 4I0) are selected when input S is LOW and the data inputs from source 1 (1I1 to 4I1) are selected when S is HIGH.

Data appears at the outputs (1 $\bar{Y}$  to 4 $\bar{Y}$ ) in inverted form from the select inputs.

The 74HC258 is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S. The outputs are forced to a high-impedance OFF-state when  $\overline{OE}$  is HIGH.

The logic equations for the outputs are:

$$1\bar{Y} = \overline{\overline{OE} \times (1I1 \times S + 1I0 \times \bar{S})}$$

$$2\bar{Y} = \overline{\overline{OE} \times (2I1 \times S + 2I0 \times \bar{S})}$$

$$3\bar{Y} = \overline{\overline{OE} \times (3I1 \times S + 3I0 \times \bar{S})}$$

$$4\bar{Y} = \overline{\overline{OE} \times (4I1 \times S + 4I0 \times \bar{S})}$$

The 74HC258 is identical to the 74HC257 but has inverting outputs.

## 2. Features

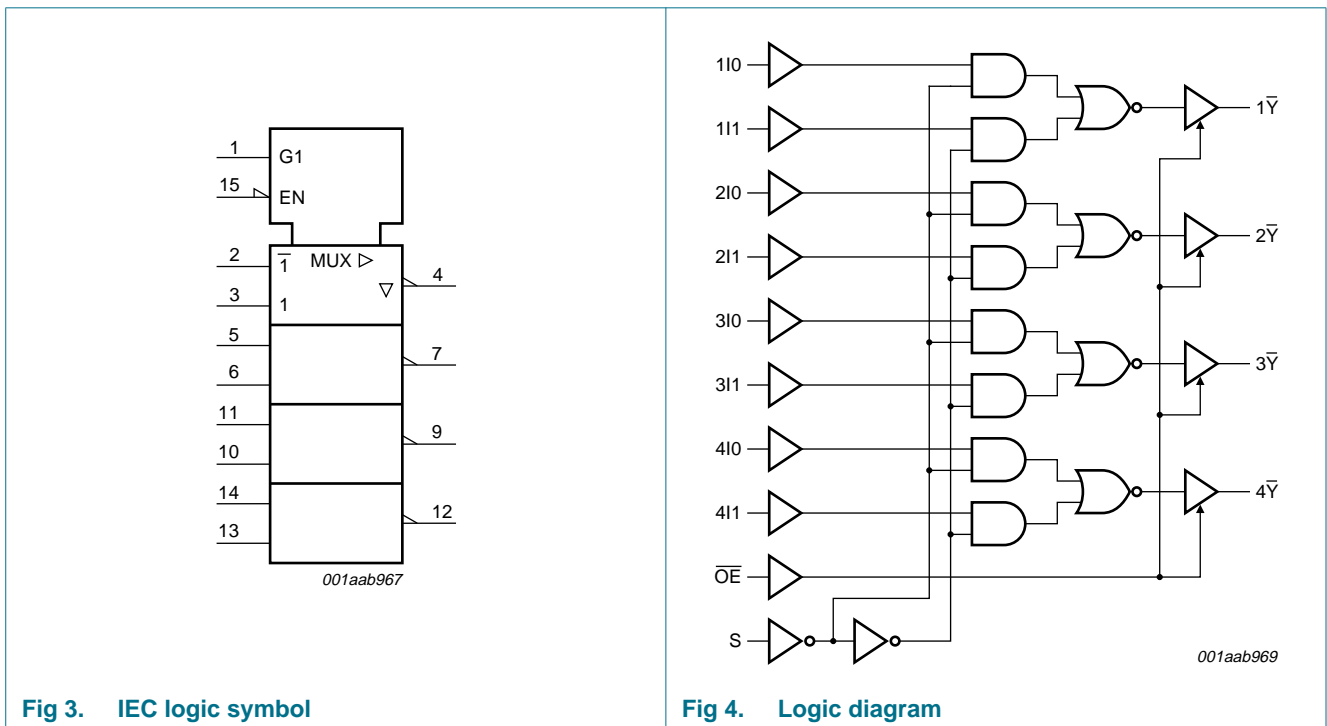
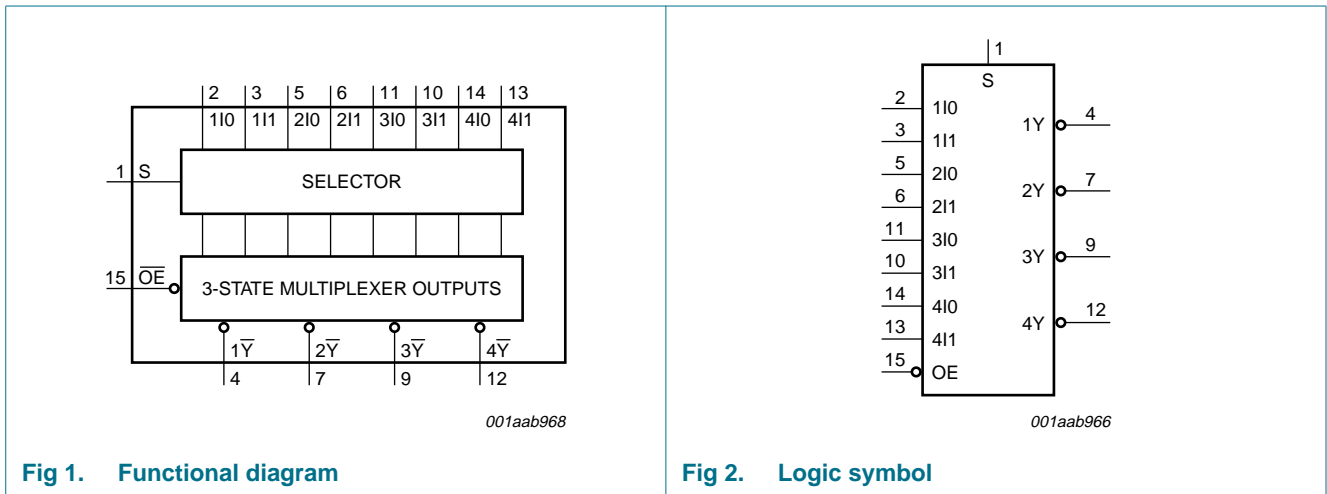
- 3-state outputs interface directly with system bus
- Low-power dissipation
- Inverting data path
- Complies with JEDEC standard no. 7A
- ESD protection:
  - ◆ HBM JESD22-A114E exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C.

### 3. Ordering information

Table 1. Ordering information

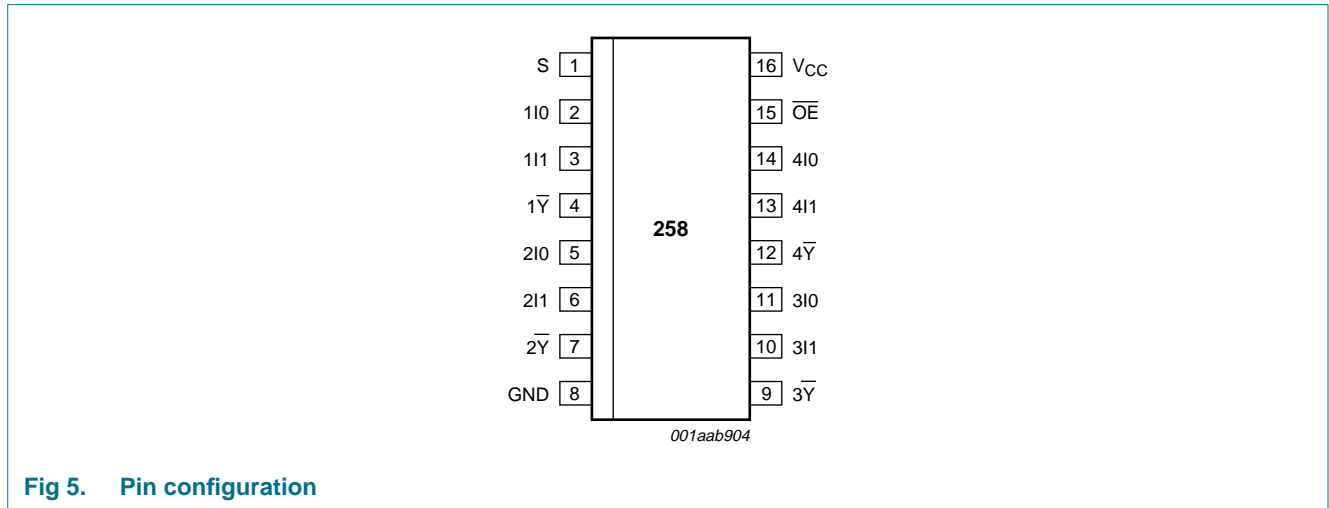
Type number	Package			Version
	Temperature range	Name	Description	
74HC258N	-40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74HC258D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC258DB	-40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1

### 4. Functional diagram



## 5. Pinning information

### 5.1 Pinning



### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
S	1	common data select input
1I0	2	data input 1 from source 0
1I1	3	data input 1 from source 1
1Y $\bar{}$	4	3-state multiplexer output 1; inverted
2I0	5	data input 2 from source 0
2I1	6	data input 2 from source 1
2Y $\bar{}$	7	3-state multiplexer output 2; inverted
GND	8	ground (0 V)
3Y $\bar{}$	9	3-state multiplexer output 3; inverted
3I1	10	data input 3 from source 1
3I0	11	data input 3 from source 0
4Y $\bar{}$	12	3-state multiplexer output 4; inverted
4I1	13	data input 4 from source 1
4I0	14	data input 4 from source 0
OE $\bar{}$	15	output enable input (active LOW)
V <sub>CC</sub>	16	positive supply voltage

## 6. Functional description

Table 3. Function table<sup>[1]</sup>

Control		Input		Output
$\overline{OE}$	S	nI0	nI1	n $\overline{Y}$
H	X	X	X	Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

- [1] H = HIGH voltage level;  
 L = LOW voltage level;  
 X = don't care;  
 Z = high-impedance OFF-state.

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	[1] -	$\pm 20$	mA
$I_{OK}$	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	[1] -	$\pm 20$	mA
$I_O$	output current	$V_O = -0.5\text{ V}$ to $V_{CC} + 0.5\text{ V}$	-	$\pm 35$	mA
$I_{CC}$	supply current		-	70	mA
$I_{GND}$	ground current		-70	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$			
		DIP16 package	[2] -	750	mW
		SO16 package	[3] -	500	mW
		SSOP16 package	[4] -	500	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 [2]  $P_{tot}$  derates linearly with 12 mW/K above 70 °C.  
 [3]  $P_{tot}$  derates linearly with 8 mW/K above 70 °C.  
 [4]  $P_{tot}$  derates linearly with 5.5 mW/K above 60 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		2.0	5.0	6.0	V
$V_I$	input voltage		0	-	$V_{CC}$	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	ns
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	ns
		$V_{CC} = 6.0\text{ V}$	-	-	83	ns

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 2.0\text{ V}$	1.5	1.2	-	1.5	-	1.5	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	2.4	-	3.15	-	3.15	-	V
		$V_{CC} = 6.0\text{ V}$	4.2	3.2	-	4.2	-	4.2	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 2.0\text{ V}$	-	0.8	0.5	-	0.5	-	0.5	V
		$V_{CC} = 4.5\text{ V}$	-	2.1	1.35	-	1.35	-	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	2.8	1.8	-	1.8	-	1.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$								
		$I_O = -20\ \mu\text{A}; V_{CC} = 2.0\text{ V}$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_O = -20\ \mu\text{A}; V_{CC} = 4.5\text{ V}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -20\ \mu\text{A}; V_{CC} = 6.0\text{ V}$	5.9	6.0	-	5.9	-	5.9	-	V
		$I_O = -6\text{ mA}; V_{CC} = 4.5\text{ V}$	3.98	4.32	-	3.84	-	3.7	-	V
		$I_O = -7.8\text{ mA}; V_{CC} = 6.0\text{ V}$	5.48	5.81	-	5.34	-	5.2	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$								
		$I_O = 20\ \mu\text{A}; V_{CC} = 2.0\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20\ \mu\text{A}; V_{CC} = 4.5\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20\ \mu\text{A}; V_{CC} = 6.0\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 6\text{ mA}; V_{CC} = 4.5\text{ V}$	-	0.15	0.26	-	0.33	-	0.4	V
		$I_O = 7.8\text{ mA}; V_{CC} = 6.0\text{ V}$	-	0.16	0.26	-	0.33	-	0.4	V
$I_I$	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0\text{ V}$	-	-	$\pm 0.1$	-	$\pm 1.0$	-	$\pm 1.0$	$\mu\text{A}$
$I_{OZ}$	OFF-state output current	$V_I = V_{IH}$ or $V_{IL}; V_{CC} = 6.0\text{ V};$ $V_O = V_{CC}$ or GND; $I_O = 0\text{ A}$	-	-	$\pm 0.5$	-	$\pm 5.0$	-	$\pm 10$	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $I_O = 0\text{ A};$ $V_{CC} = 6.0\text{ V}$	-	-	8	-	80	-	160	$\mu\text{A}$
$C_I$	input capacitance		-	3.5	-	-	-	-	-	pF

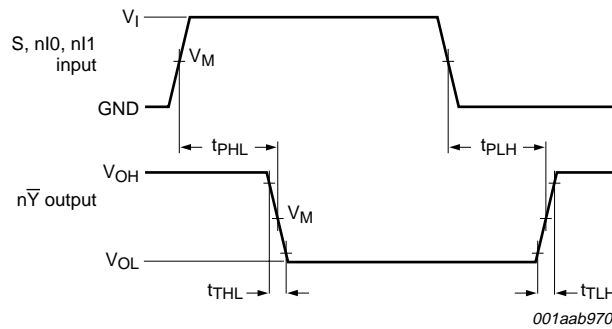
## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**  
*GND = 0 V; for test circuit see Figure 8.*

Symbol	Parameter	Conditions	25 °C			-40 °C to +125 °C		Unit	
			Min	Typ	Max	Max (85 °C)	Max (125 °C)		
$t_{pd}$	propagation delay	nI0, nI1to n $\bar{Y}$ ; see <a href="#">Figure 6</a> <a href="#">[1]</a>							
		$V_{CC} = 2.0\text{ V}$	-	30	95	120	145	ns	
		$V_{CC} = 4.5\text{ V}$	-	11	19	24	29	ns	
		$V_{CC} = 6.0\text{ V}$	-	9	16	20	25	ns	
		$V_{CC} = 5.0\text{ V}; C_L = 15\text{ pF}$	-	9	-	-	-	ns	
		S to n $\bar{Y}$ ; see <a href="#">Figure 6</a>							
		$V_{CC} = 2.0\text{ V}$	-	47	140	175	210	ns	
		$V_{CC} = 4.5\text{ V}$	-	17	28	35	42	ns	
		$V_{CC} = 6.0\text{ V}$	-	14	24	30	36	ns	
		$V_{CC} = 5.0\text{ V}; C_L = 15\text{ pF}$	-	14	-	-	-	ns	
$t_{en}$	enable time	$\overline{OE}$ to n $\bar{Y}$ ; see <a href="#">Figure 7</a> <a href="#">[2]</a>							
		$V_{CC} = 2.0\text{ V}$	-	39	140	175	210	ns	
		$V_{CC} = 4.5\text{ V}$	-	14	28	35	42	ns	
		$V_{CC} = 6.0\text{ V}$	-	11	24	30	36	ns	
$t_{dis}$	disable time	$\overline{OE}$ to n $\bar{Y}$ ; see <a href="#">Figure 7</a> <a href="#">[3]</a>							
		$V_{CC} = 2.0\text{ V}$	-	55	150	190	225	ns	
		$V_{CC} = 4.5\text{ V}$	-	20	30	38	45	ns	
		$V_{CC} = 6.0\text{ V}$	-	16	26	33	38	ns	
$t_t$	transition time	see <a href="#">Figure 6</a> <a href="#">[4]</a>							
		$V_{CC} = 2.0\text{ V}$	-	14	60	75	90	ns	
		$V_{CC} = 4.5\text{ V}$	-	5	12	15	18	ns	
		$V_{CC} = 6.0\text{ V}$	-	4	10	13	15	ns	
$C_{PD}$	power dissipation capacitance	per multiplexer; $V_I = \text{GND to } V_{CC}$	<a href="#">[5]</a>	-	55	-	-	-	pF

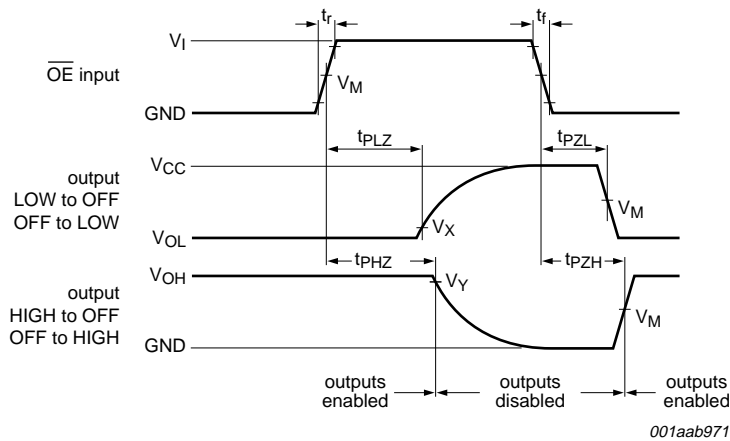
- [1]  $t_{pd}$  is the same as  $t_{PHL}$  and  $t_{PLH}$ .
- [2]  $t_{en}$  is the same as  $t_{PZH}$  and  $t_{PZL}$ .
- [3]  $t_{dis}$  is the same as  $t_{PHZ}$  and  $t_{PLZ}$ .
- [4]  $t_t$  is the same as  $t_{THL}$  and  $t_{TLH}$ .
- [5]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  
 $f_o$  = output frequency in MHz;  
 $C_L$  = output load capacitance in pF;  
 $V_{CC}$  = supply voltage in V;  
 $N$  = number of inputs switching;  
 $\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

11. Waveforms



Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig 6. Input (nI0, nI1 and S) to output (nY) propagation delays and output transition times**

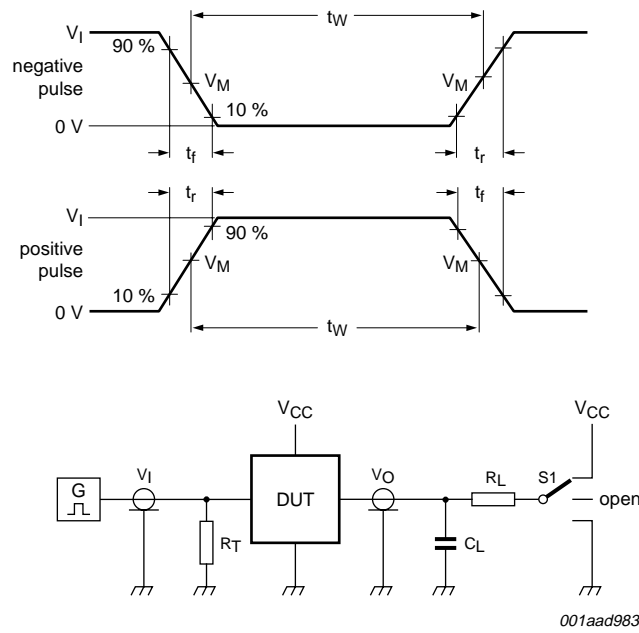


Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig 7. Enable and disable times**

**Table 8. Measurement points**

Input	Output		
$V_M$	$V_M$	$V_X$	$V_Y$
$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$0.1 \times V_{CC}$	$0.9 \times V_{CC}$



Test data is given in [Table 9](#).

Definitions test circuit:

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_L$  = Load resistance.

S1 = Test selection switch.

**Fig 8. Test circuit for measuring switching times**

**Table 9. Test data**

Supply voltage	Input		Load		S1		
$V_{CC}$	$V_I$	$t_r = t_f$	$C_L$	$R_L$	$t_{PZL}, t_{PLZ}$	$t_{PZH}, t_{PHZ}$	$t_{PHL}, t_{PLH}$
2.0 V	$V_{CC}$	6 ns	50 pF	1 k $\Omega$	$V_{CC}$	GND	open
4.5 V	$V_{CC}$	6 ns	50 pF	1 k $\Omega$	$V_{CC}$	GND	open
6.0 V	$V_{CC}$	6 ns	50 pF	1 k $\Omega$	$V_{CC}$	GND	open
5.0 V	$V_{CC}$	6 ns	15 pF	1 k $\Omega$	$V_{CC}$	GND	open



12. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4

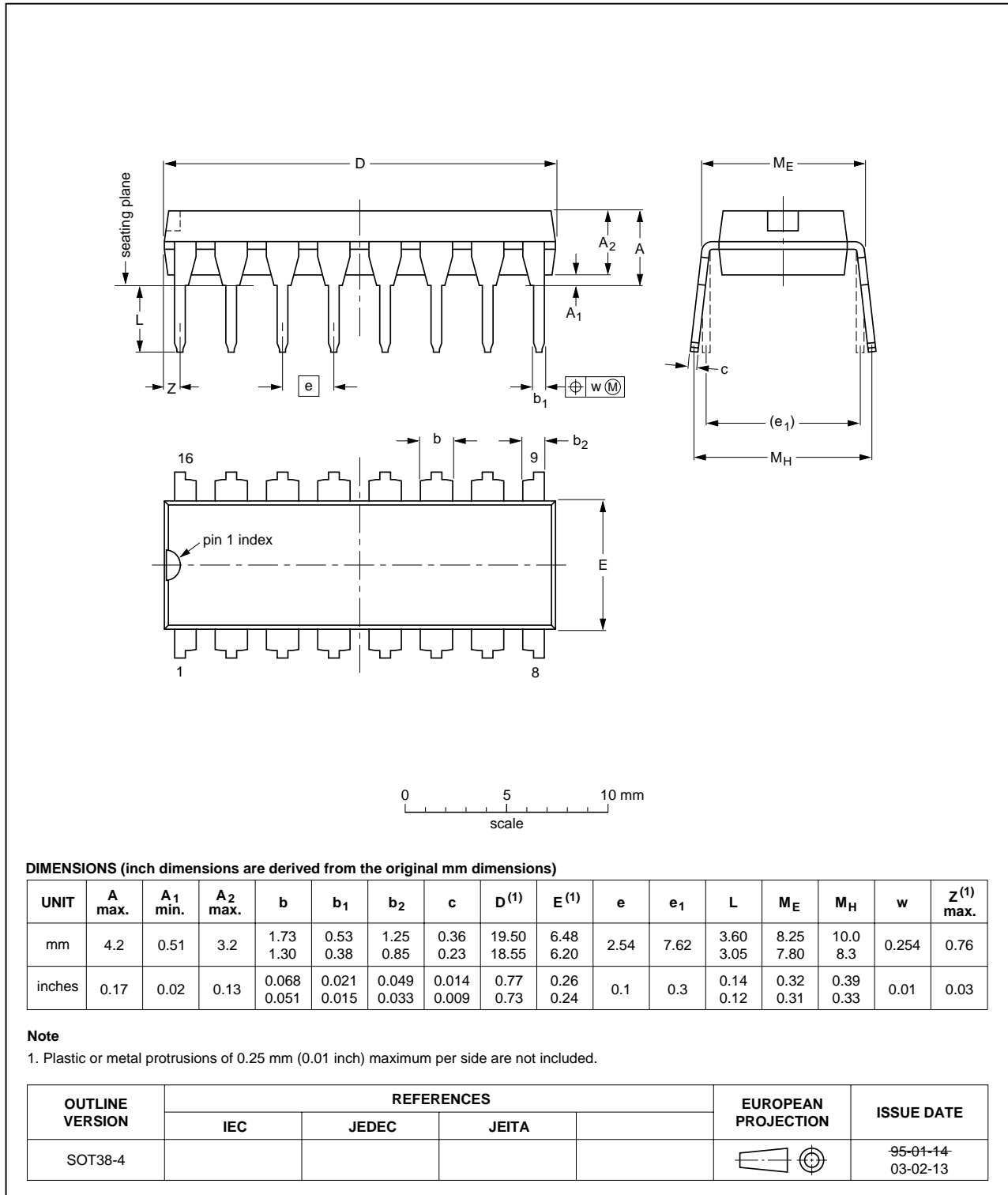


Fig 9. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

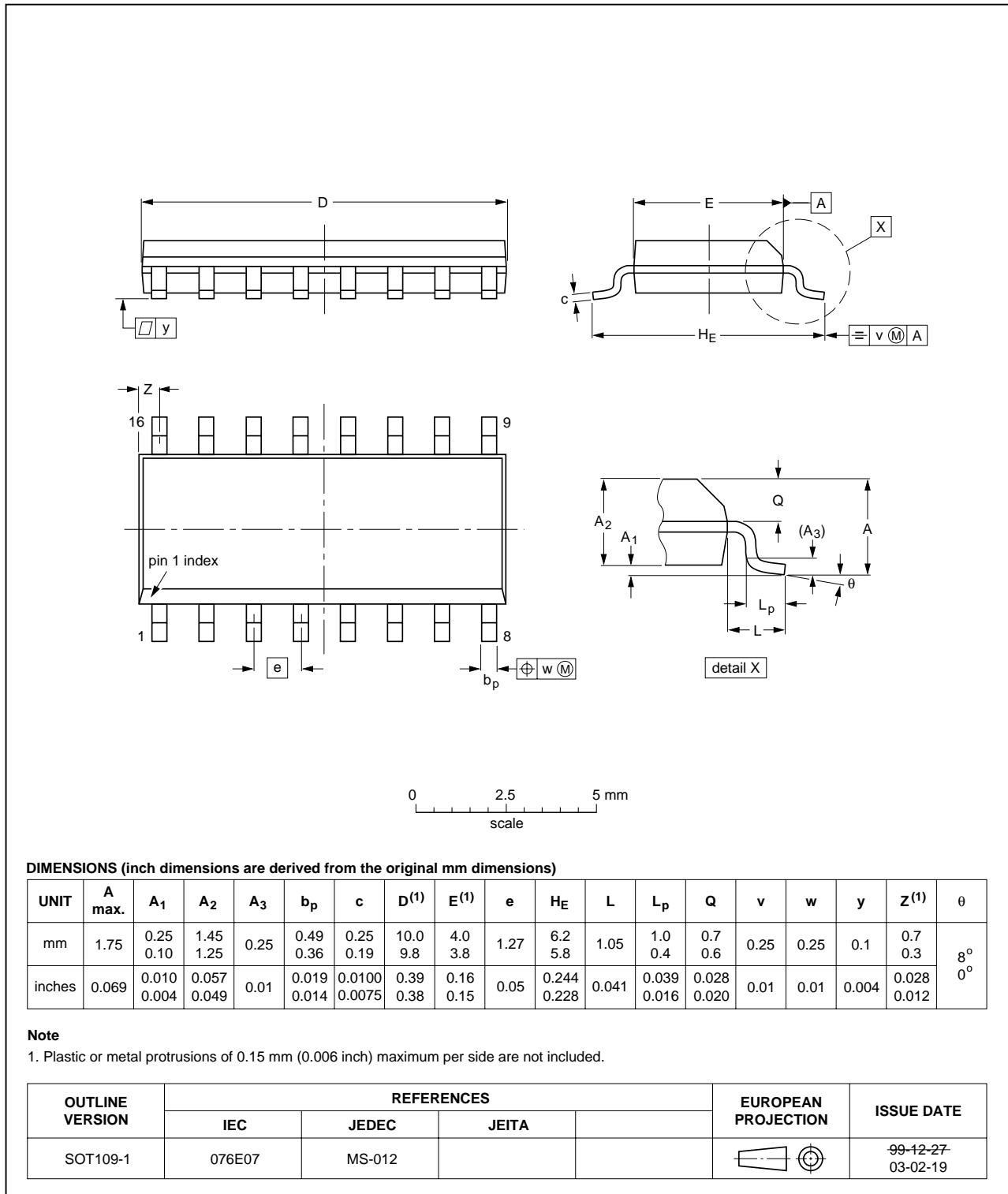


Fig 10. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

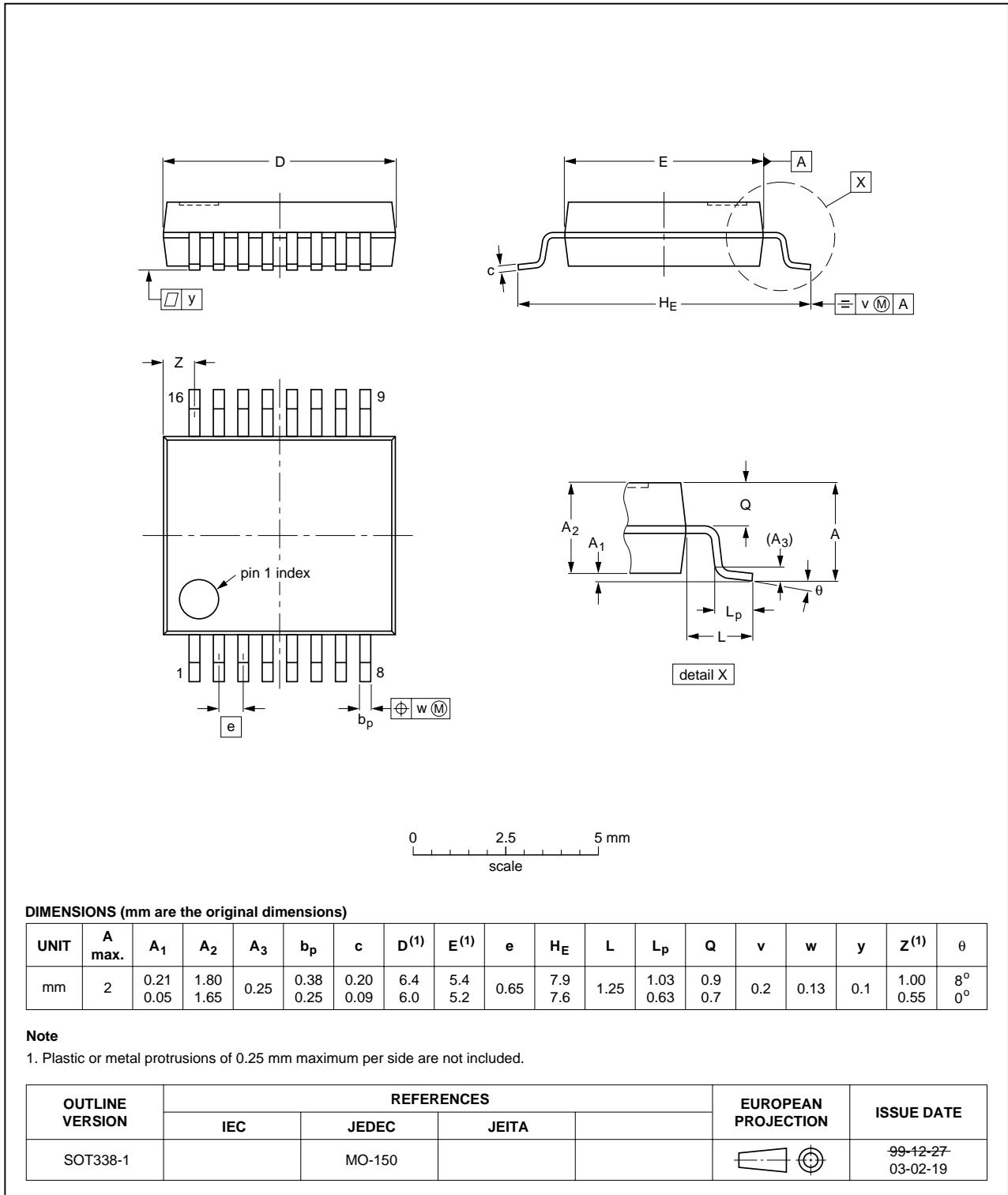


Fig 11. Package outline SOT338-1 (SSOP16)

## 13. Abbreviations

**Table 10. Abbreviations**

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

**Table 11. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC258_4	20080414	Product data sheet	-	74HC258_3
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Pin assignment corrected for pins 10, 11, 13 and 14 in <a href="#">Figure 1</a>, <a href="#">Figure 2</a>, <a href="#">Figure 5</a> and <a href="#">Table 2</a>.</li> </ul>			
74HC258_3	20041112	Product data sheet	-	74HC_HCT258_CNV_2
74HC_HCT258_CNV_2	19990902	Product specification	-	74HC_HCT258_1
74HC_HCT258_1	19901201	Product specification	-	-

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### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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